Applicant gratefully acknowledges the allowance of claim 65.[1]

Claims 29-32, 34-39, 41, 44-47, 49 and 51-64 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Wetzel (U.S. Patent No. 6,143,646) ("Wetzel") in view of Aoki et al. (U.S. Patent No. 6,033,953) ("Aoki"). This rejection is respectfully traversed and reconsideration is respectfully requested.

The claimed invention relates to an electropolished patterned metal layer formed as a lower electrode of a capacitor, which may be part of a semiconductor device, such as a memory cell, or a processor-based system. The electropolished metal layer of the claimed invention allows for high resolution patterning with increased processing accuracy in the patterning of noble metals. Specification, page 8, lines 5-10. As shown in FIG. 14 (reproduced below for convenience), the electropolished lower electrode 70 is formed such that it is fully within a contact opening (41, FIG. 7) within insulating layer 25. The capacitor 100 may also include a barrier conductive layer 60 between the insulating layer 25 and the lower electrode 70. A dielectric layer 72 is formed over the lower electrode 70. Upper electrode 74 is formed over dielectric layer 72.

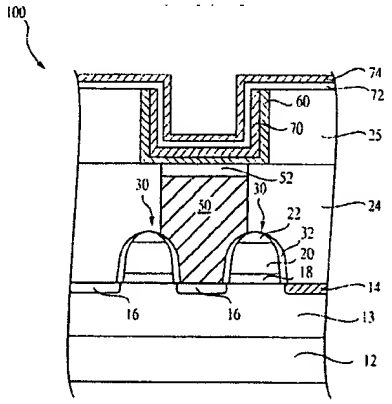

FIG. 14

[1] Applicant notes that the Examiner's comments on the reasons for allowance of claim 65 do not correspond to claim 65, but are the same comments that were previously given with respect to claim 29, the allowance of which has been withdrawn by the current Office Action.

Claim 36 recites a memory cell comprising a "transistor including a gate fabricated on a semiconductor substrate and including a source/drain region in said semiconductor substrate disposed adjacent to said gate," an "insulating layer provided over said substrate" and a "container capacitor." The capacitor includes a "lower electrode, a dielectric layer over said lower electrode, and an upper electrode over said dielectric layer, said upper electrode comprising doped polysilicon, and said lower electrode having a surface aligned over said source/drain region." The "lower electrode comprises an electropolished patterned metal layer which is situated fully within said insulating layer [and] ... has a thickness of about 50 to about 300 Angstroms." Further, the "dielectric layer is in contact with said insulating layer."

Claim 44 recites a processor-based system including a "processor" and an "integrated circuit coupled to said processor." Further, "at least one of said integrated circuit and said processor compris[e] a container capacitor provided within an insulating layer, said container capacitor including a lower electrode and an upper electrode, said lower electrode comprising an electropolished patterned metal layer having a thickness of approximately 50 to 300 Angstroms, wherein a top surface of said electropolished patterned metal layer is at the same level with a top surface of said insulating layer such that said lower electrode does not extend above the top surface of said insulating layer."

Claim 55 recites a container capacitor including a "lower electrode provided fully within a first insulating layer, said lower electrode comprising an electropolished patterned metal layer having a bottom wall and vertical sidewalls extending rectangularly upwardly therefrom," a "second insulating layer provided over said electropolished patterned metal layer and in contact with said first insulating layer" and an "upper electrode provided over said second insulating layer."

Claim 59 recites a container capacitor including an "insulating layer provided over a substrate, said insulating layer containing an opening," a "tantalum nitride barrier conductive layer provided at a bottom of said opening," a "lower electrode provided over said tantalum

nitride barrier conductive layer, said lower electrode comprising an electropolished patterned metal layer having a bottom and vertical sidewalls extending upwardly from said bottom such that said lower electrode is situated fully within said insulating layer, said lower electrode having a thickness of approximately 100 Angstroms," a "dielectric material provided over said electropolished patterned metal layer and in contact with said insulating layer" and an "upper electrode comprising doped polysilicon provided over said dielectric material." The "lower electrode, said dielectric material and said upper electrode form said container capacitor."

Claim 60 recites a container capacitor structure including an "insulating layer provided over a substrate," a "plurality of openings provided in said insulating layer," a "plurality of lower capacitor electrodes provided along the bottom and sidewalls of respective ones of said openings, said lower electrodes being formed as discrete electropolished metal layers such that said lower electrodes do not extend above an upper surface of said insulating layer" and a "dielectric layer associated with each of said discrete lower electrodes, said dielectric layer being in contact with said insulating layer."

Claim 29 recites an intermediate semiconductor device structure[2] comprising a "substrate," an "insulating layer provided over said substrate," an "electropolished patterned metal layer provided within an opening of said insulating layer," and a "photoresist plug provided within said opening and over and in contact with said electropolished patterned metal layer." The "electropolished metal layer has a thickness of approximately 50 to 300 Angstroms." Also, a "top surface of said electropolished metal layer is electropolished down to said insulating layer so that said top surface of said electropolished metal layer is at the same level with a top surface of said insulating layer."

In order to establish a *prima facie* case of obviousness "the prior art reference (or references when combined) must teach or suggest all the claim limitations." M.P.E.P. § 2142. Applicant respectfully submits that the Office Action fails to set forth a *prima facie* case of

[2] The intermediate structure of claim 29 can be seen, for example, in FIG. 12.

obviousness. Applicant submits that the combination of Wetzel and Aoki does not disclose, teach or suggest all the limitations of the claimed invention.

First of all, Applicant respectfully points out that this is essentially the same rejection contained in the Office Action dated July 26, 2007 (and in the Office Action of January 25, 2007). The allowance of claims 29-32, 34 and 35 has been withdrawn, however, no discussion of these claims is included in the rejection. Further, it appears as if the only difference between the current Office Action and the one dated July 26, 2007 is that the reference previously cited has been replaced by Wetzel. However, the discussion of the rejection is exactly the same.

Wetzel relates to a method for forming a dual inlaid contact structure (damascene) by etching dual inlaid contact structures with the deposition of low-K dielectric material to selectively form low-K regions only in critical areas where low-K dielectric material is absolutely needed. Wetzel, Abstract. Other portions of the wafer remain covered with conventional oxide so that adverse impacts of low-K dielectric material is minimized. Id. Conductive material is then formed to complete dual inlaid contact structures whereby low-K dielectric plugs reduce cross talk and capacitance within the final structure. Id.

As can be seen in FIG. 30 (reproduced below for convenience), low-K dielectric region 530 is positioned within the critical area between inlaid metal regions 512a/512b. Barrier layer 508 isolates metal regions 510/512 from the adjacent oxide layers.

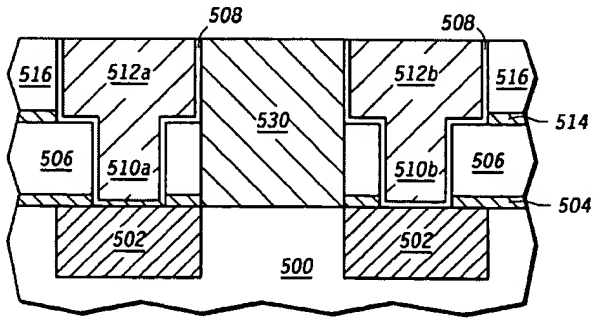

FIG. 30

The combination of Wetzel and Aoki fails to disclose all of the limitations of the claimed invention. Even assuming that the Office Action asserts that Wetzel's barrier layer 508 (Figure 30) discloses the claimed lower electrode (electropolished patterned metal layer) the cited combination of references does not disclose the "dielectric layer over [the] lower electrode" of claim 36, the processor of claim 44, the claimed "container capacitor," of claims 36 and 44, the "second insulating layer provided over [the] electropolished patterned metal layer" of claim 55, the "dielectric layer ... in contact with [the] insulating layer" of claim 60, or the "upper electrode" of claims 36, 44, 55, 59 and dependent claim 61. The cited combination of references also fails to disclose an intermediate structure including a "substrate," an "insulating layer provided over said substrate," an "electropolished patterned metal layer provided within an opening of said insulating layer," and a "photoresist plug provided within said opening and over and in contact with said electropolished patterned metal layer," as recited by claim 29.

There is no indication in the Office Action with respect to which portions of Figure 30 of Wetzel allegedly correspond to different portions of the claims. The Office has failed to satisfy its burden under the MPEP 37 CFR 1.104[3] and adequately describe how the claimed invention is disclosed by the cited combination of references.

Aoki relates to a method of forming a dielectric capacitor with a reduced leakage current. Aoki, Abstract. Aoki is relied upon as disclosing the use of platinum as a material for forming the lower electrode by using an electropolishing method (Office Action, page 3), but does not remedy the deficiencies of Wetzel as to the undisclosed limitations previously discussed.

[3] 37 CFR 1.104 Nature of examination "(c) Rejection of claims...
(2) In rejecting claims for want of novelty or for obviousness, the examiner must cite the best references at his or her command. When a reference is complex or shows or describes inventions other than that claimed by the applicant, the particular part relied on must be designated as nearly as practicable. The pertinence of each reference, if not apparent, must be clearly explained and each rejected claim specified."

Moreover, Applicant submits that the Office Action has not properly shown that the Applicant's claims would have been obvious by conducting an examination of the Graham factors. "Patent examiners carry the responsibility of making sure that the standard of patentability enunciated by the Supreme Court and by the Congress is applied in each and every case." M.P.E.P. § 2141. Instead, to show that Wetzel and Aoki may be properly combined and that the Applicant's claims are obvious in light of these references, the Office Action merely stated that it would be obvious to use the electropolishing method of Aoki for forming the electropolished patterned metal layer of Wetzel because such electropolishing method for forming the electropolished patterned metal layer would "reduce the leakage current of the capacitor" (Office Action at pages 3 and 4) and would "decrease the processability and the electric current distribution becomes nonuniform" (Office Action at pages 5 and 6). These statements are not an adequate substitution for an analysis of the Graham factors and do not show that it would have been obvious to combine the two references. Further, the Office Action does not even point to what portion of Wetzel is the alleged "patterned metal layer" which would be obvious to form by the method of Aoki.

Accordingly, claims 29, 36, 44, 55, 59 and 60 are allowable over the cited combination. Claims 30-32, 34 and 35 depend from claim 29 and are allowable along with claim 29. Claims 37-39 and 41 depend from claim 36 and are allowable along with claim 36. Claims 45-47, 49 and 51-54 depend from claim 44 and are allowable along with claim 44. Claims 56-58 depend from claim 55 and are allowable along with claim 55. Claims 61-64 depend from claim 60 and are allowable along with claim 60. Applicant respectfully requests that the rejection of claims 36-39, 41, 44-47, 49 and 51-64 be withdrawn and the claims allowed.

In view of the above, Applicant believes the pending application is in condition for allowance.

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Respectfully submitted,

By _____ #41,198

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